(12) UK Patent Application (19) GB (11) 2 295 060 (13) A

(43) Date of A Publication 15.05.1996

(21) Application No 9422140.5

(22) Date of Filing 02.11.1994

(51) INT CL[6]
H03K 3/017 , H03L 7/08

(52) UK CL (Edition O)
H3A AP ASX
U1S S1990

(56) Documents Cited
US 4743783 A

(58) Field of Search
UK CL (Edition N) H3A ASX AXX , H3P PKGW
INT CL[6] H03K , H03L
Online: WPI, EDOC, JAPIO, INSPEC

(71) Applicant(s)
Perkins Limited

(Incorporated in the United Kingdom)

Eastfield, PETERBOROUGH, Cambridgeshire, PE1 5NA, United Kingdom

(72) Inventor(s)
Colin John Wilson

(74) Agent and/or Address for Service
Fitzpatricks
Cardinal Court, 23 Thomas More Street, LONDON, E1 9YY, United Kingdom

(54) PLL control of pulse width modulation

(57) The control arrangement comprises a circuit for generating a nominally constant off-time pwm drive signal from an inputted pwm source signal, a phase comparator for comparing the phase of the inputted pwm source signal with the phase of a signal in said nominally constant off-time circuit; output of the phase comparator is connected to a control input of a generator of said constant off-time circuit to vary the pulse duration of the generator in order to lock the phase of an output signal of the generator with a predetermined point in each cycle of the pwm source signal. In the PWM drive circuit, an integrated output of the PWM source signal at G is compared with the voltage across source resistor Rs for turning a latch off which is turned on again after a fixed duration via a monostable circuit. The duration of this monostable period is controllable via the phase locked loop to ensure synchronisation of the PWM drive signal with the PWM source signal.

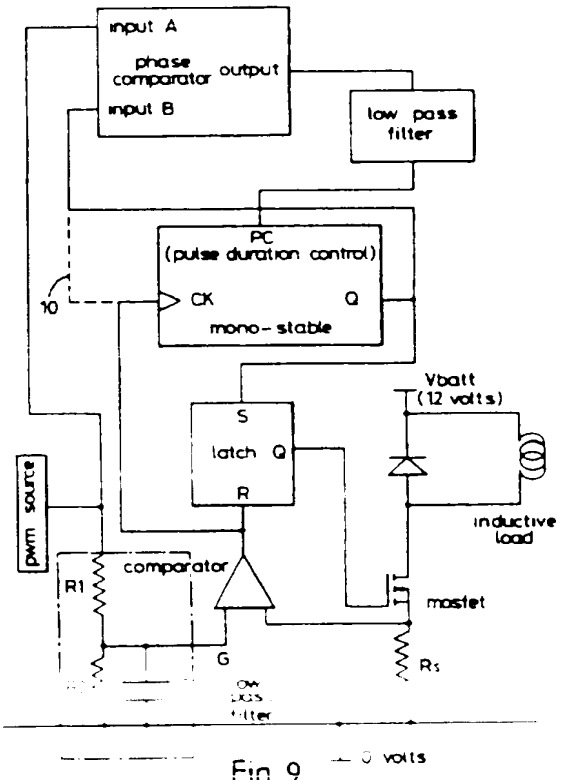

Fig. 9

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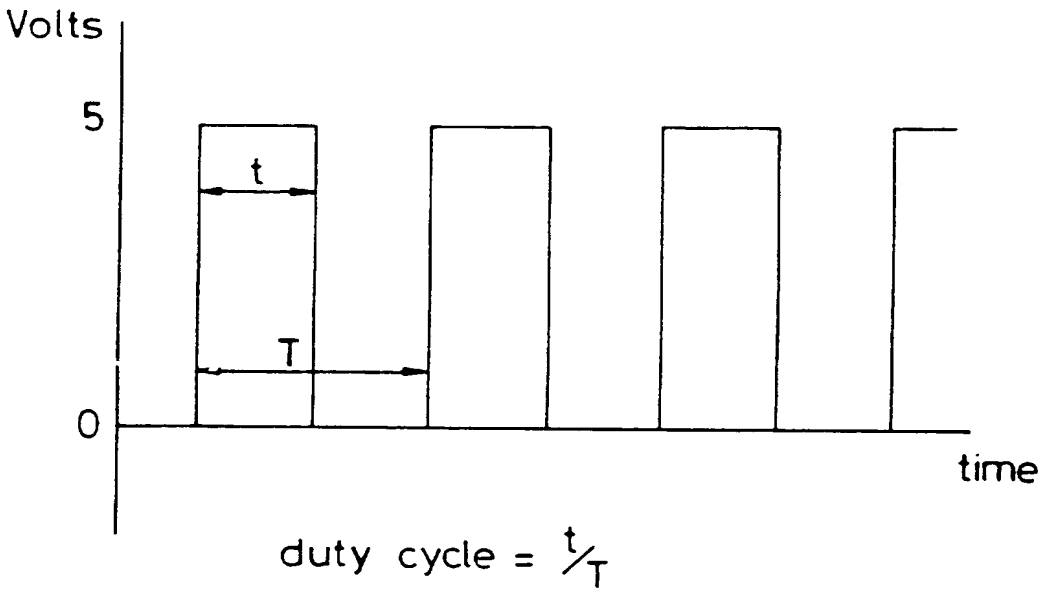
Volts
5
0
t
T
time
duty cycle = t/T

Fig. 1

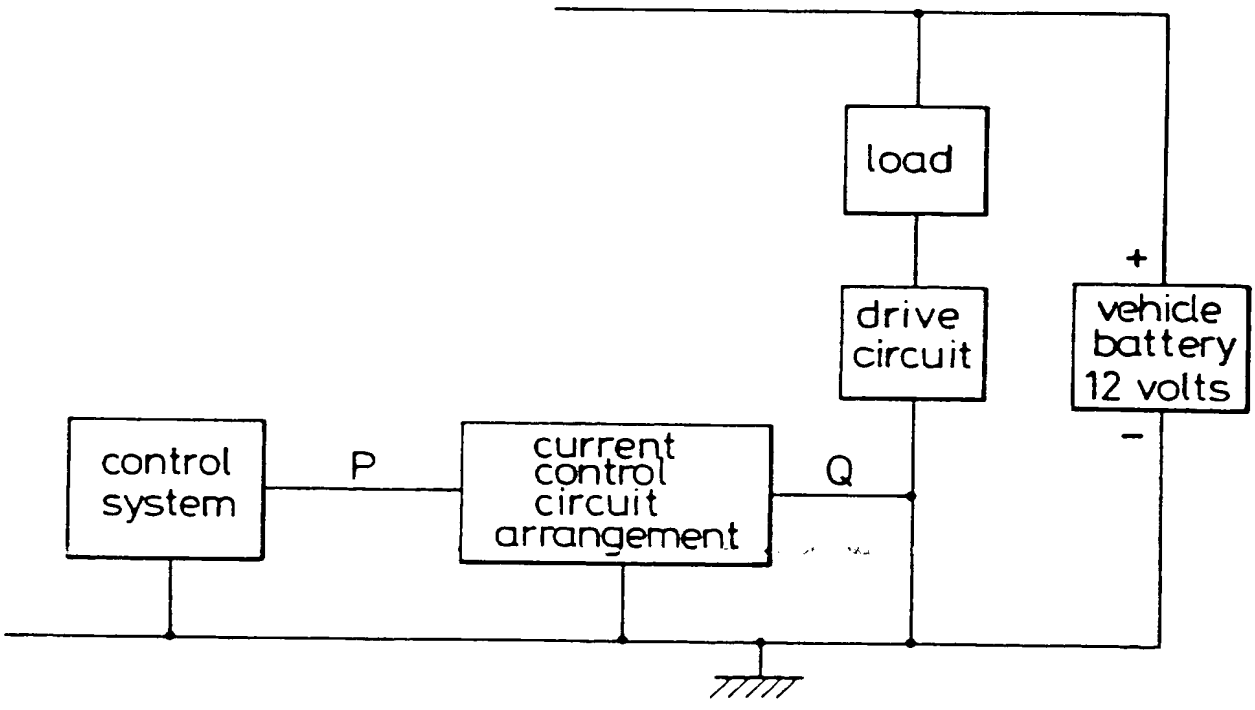
load
drive circuit
+
vehicle battery 12 volts
−
control system
P
current control circuit arrangement
Q

Fig. 2

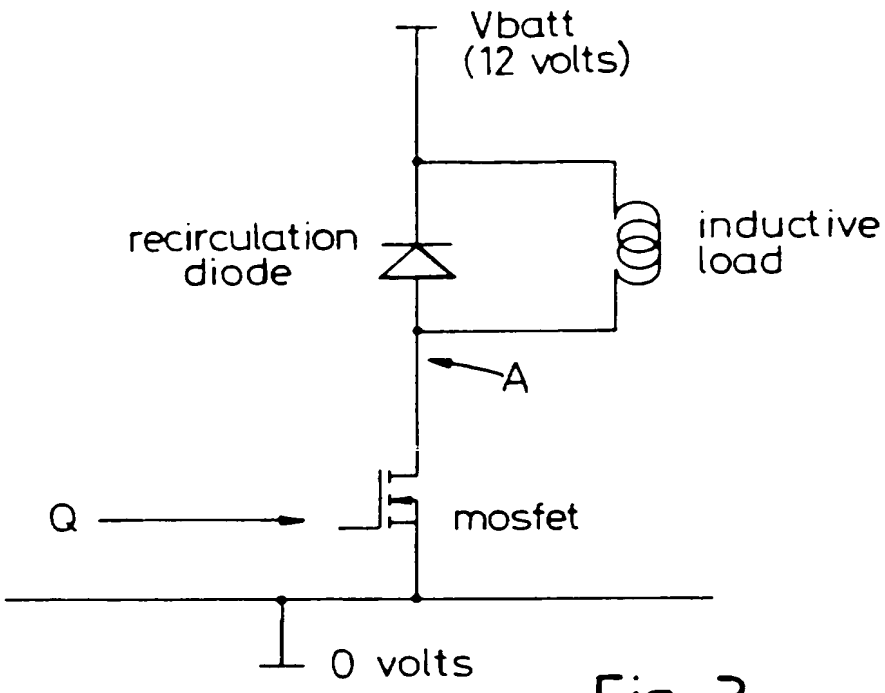
Vbatt
(12 volts)
recirculation
diode
inductive
load
A
Q
mosfet
0 volts

Fig. 3

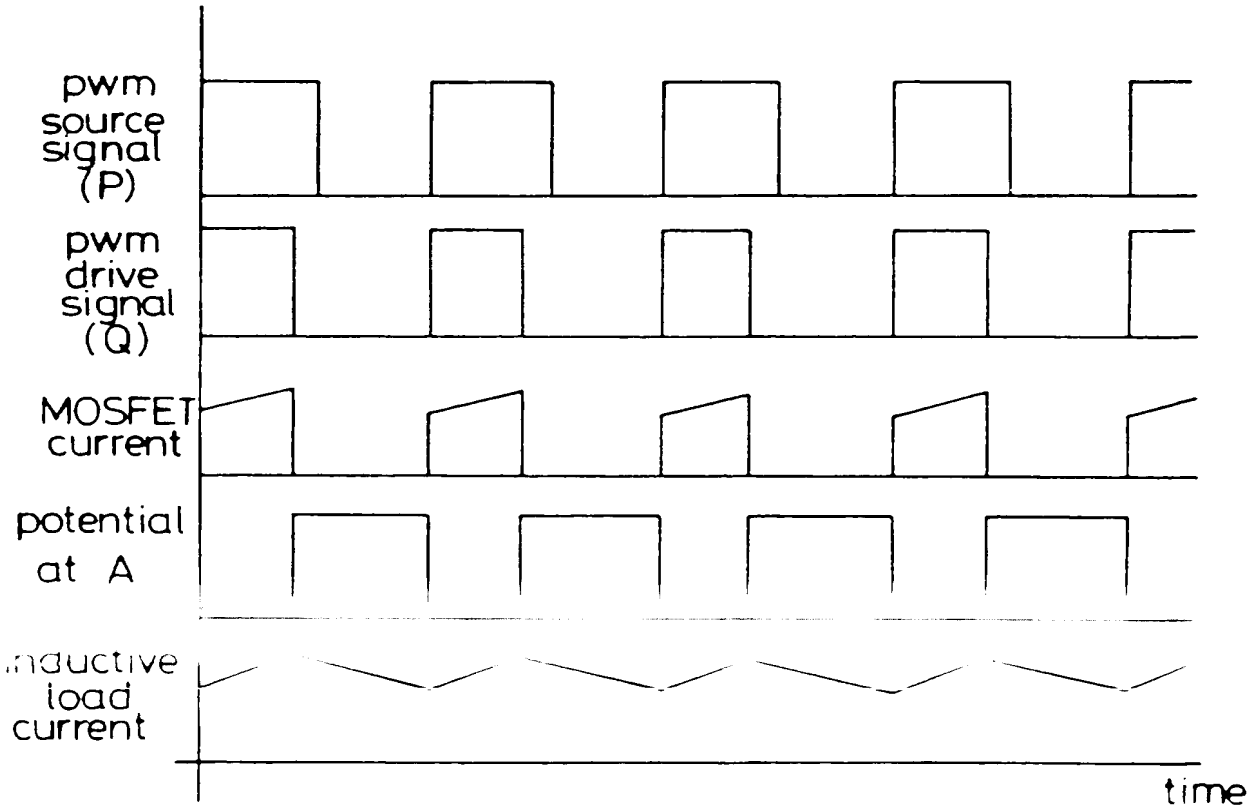
pwm
source
signal
(P)
pwm
drive
signal
(Q)
MOSFET
current
potential
at A
inductive
load
current
time

Fig. 4

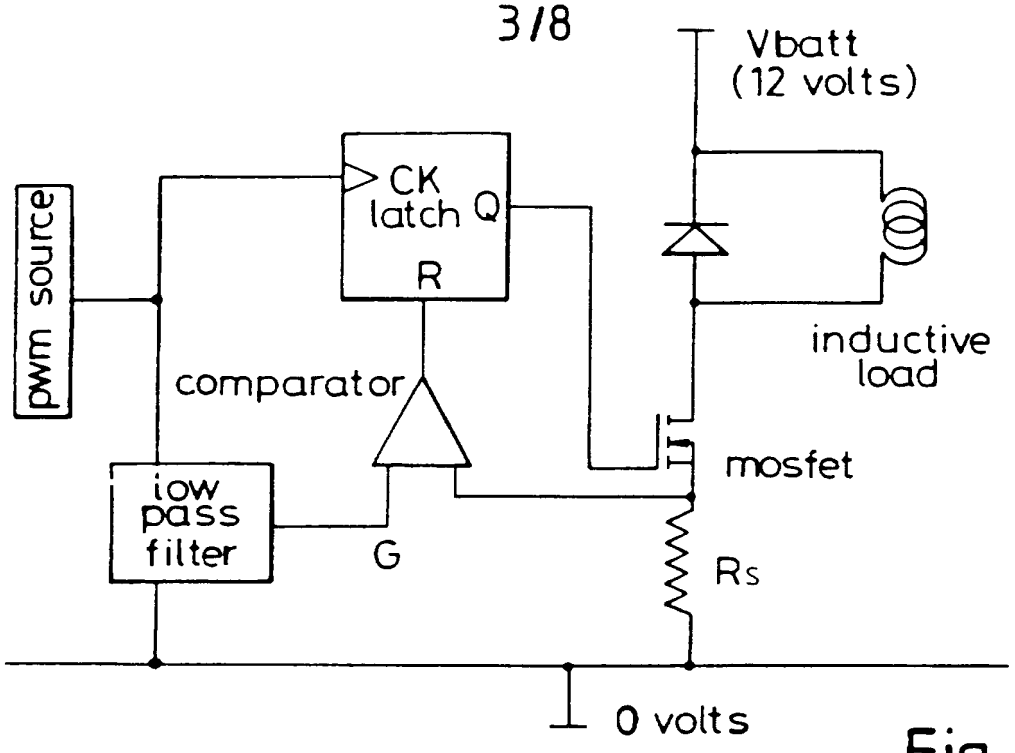
Vbatt
(12 volts)
CK
latch Q
R
pwm source
comparator
inductive
load
mosfet
low
pass
filter
G
Rs
0 volts

Fig. 5

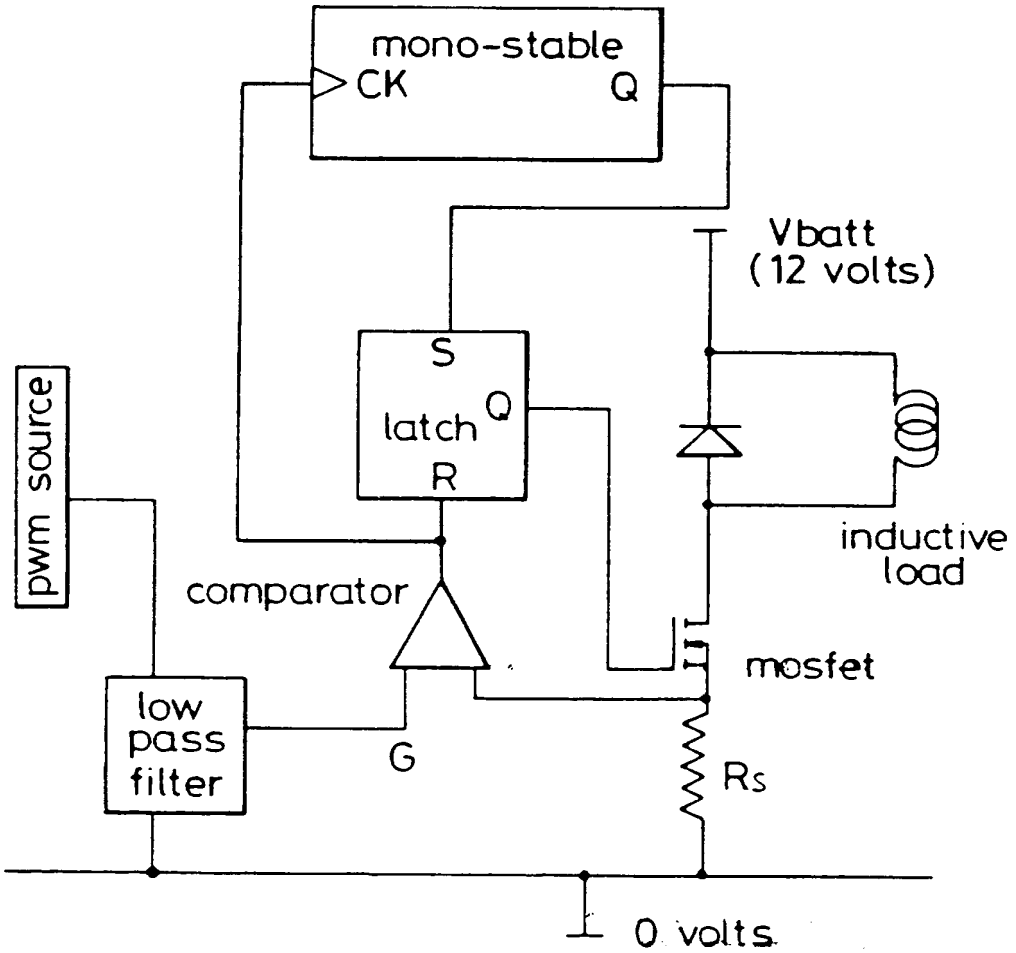
mono-stable
CK
Q
Vbatt
(12 volts)
S
latch Q
R
pwm source
inductive
load
comparator
mosfet
low
pass
filter
G
Rs
0 volts

Fig. 6

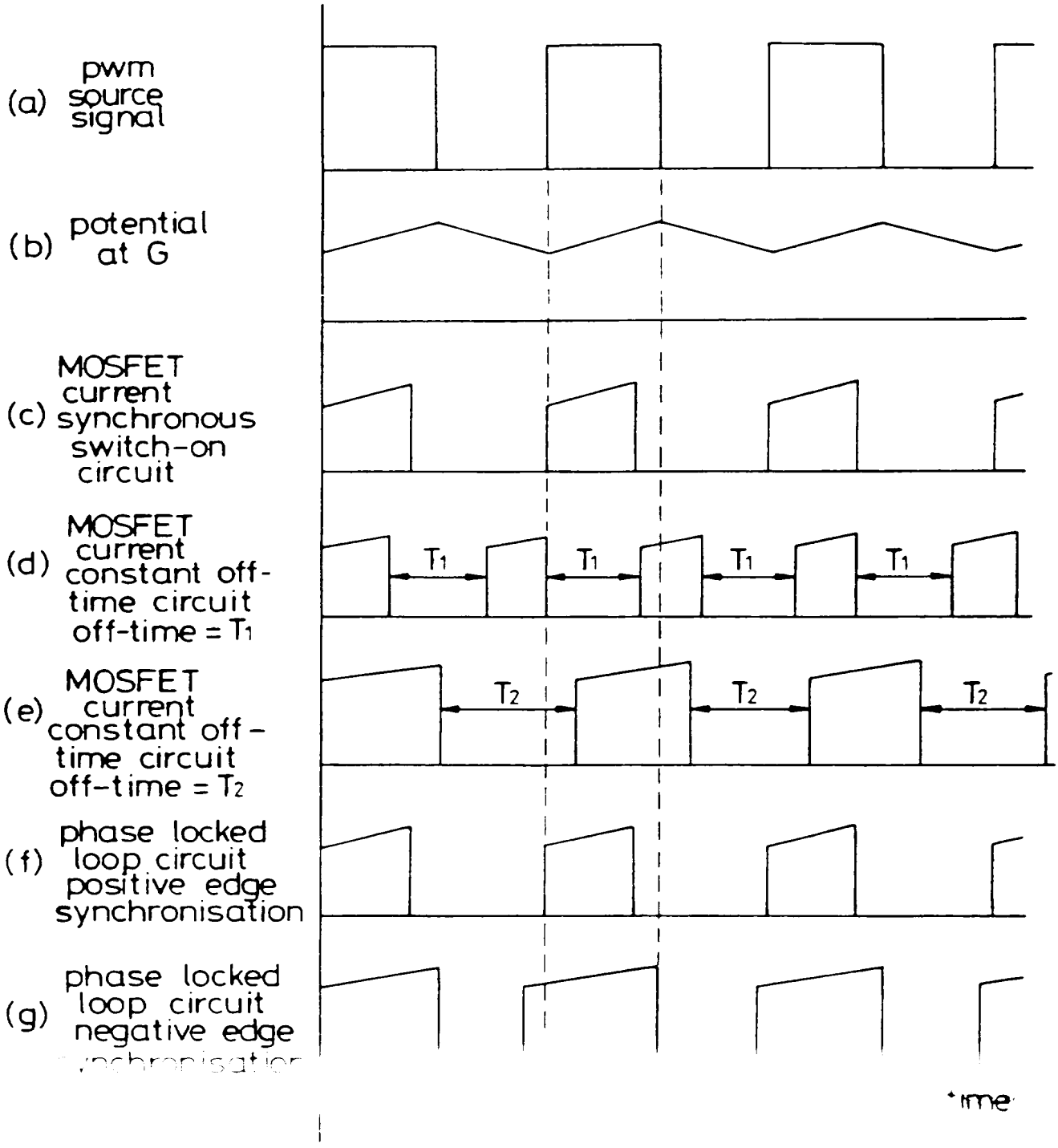
(a) pwm source signal
(b) potential at G
(c) MOSFET current synchronous switch-on circuit
(d) MOSFET current constant off-time circuit off-time = T1
(e) MOSFET current constant off-time circuit off-time = T2
(f) phase locked loop circuit positive edge synchronisation
(g) phase locked loop circuit negative edge synchronisation
T1
T2
time

Fig. 7

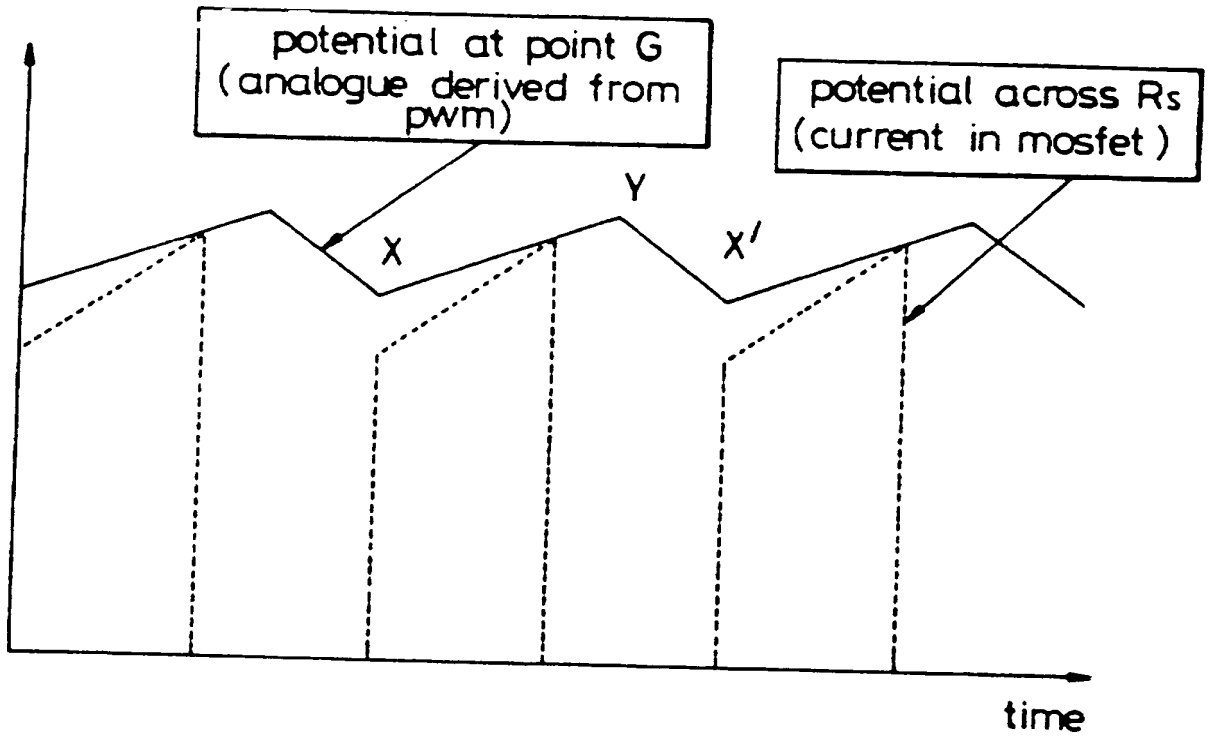

Fig. 8

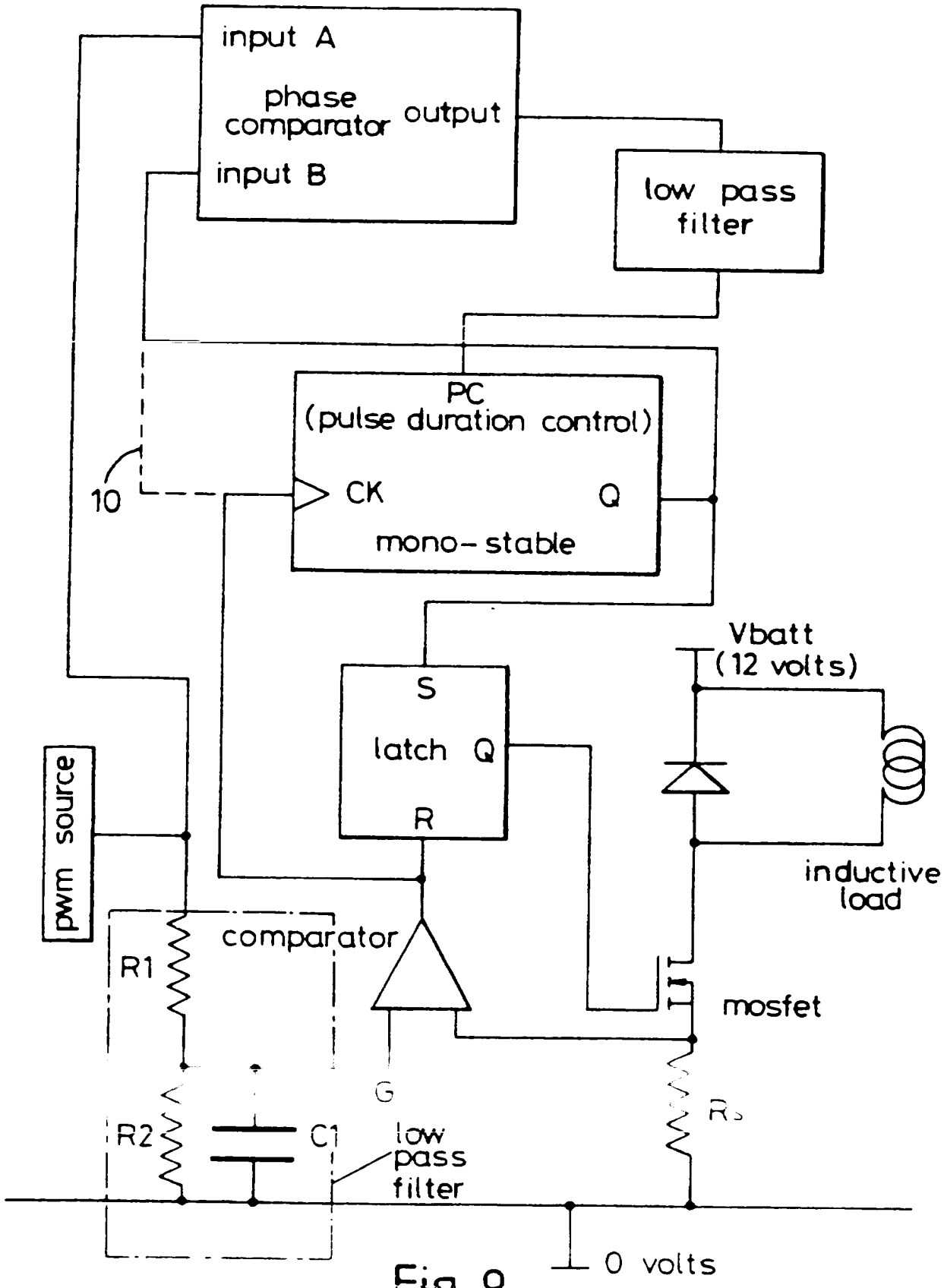
input A
phase comparator
output
input B
low pass filter
PC
(pulse duration control)
CK
Q
mono-stable
10
Vbatt
(12 volts)
S
latch Q
R
pwm source
inductive load
comparator
R1
mosfet
G
R2
C1
low pass filter
0 volts

Fig. 9

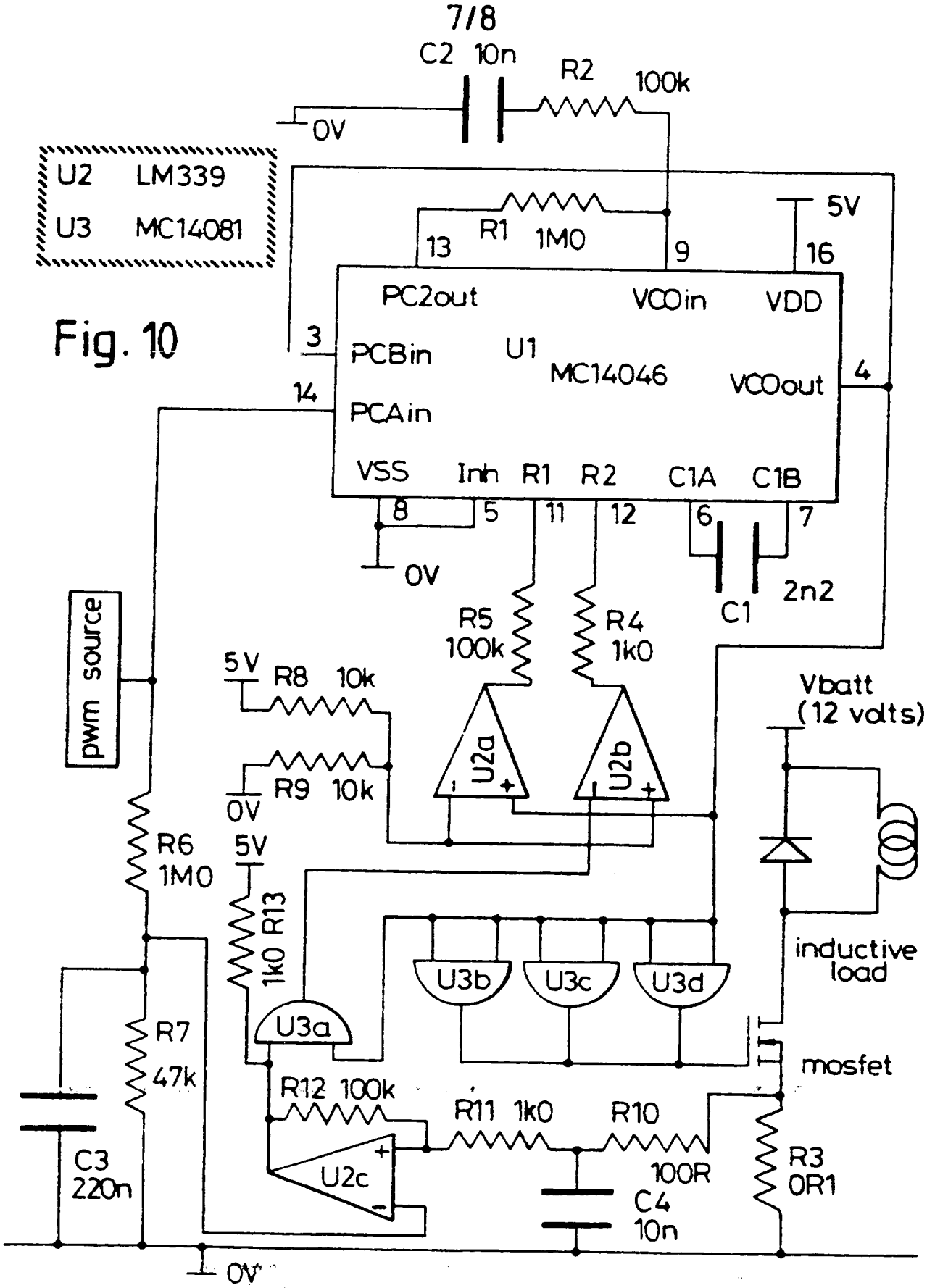
C2 10n
R2 100k
0V
U2 LM339
U3 MC14081
R1 1M0
5V
13
9
16
PC2out
VCOin
VDD
3
PCBin
U1
MC14046
VCOout
4
14
PCAin
VSS
Inh
R1
R2
C1A
C1B
8
5
11
12
6
7
0V
C1
2n2
R5 100k
R4 1k0
pwm source
5V
R8 10k
R9 10k
0V
U2a
U2b
Vbatt (12 volts)
R6 1M0
5V
1k0 R13
U3b
U3c
U3d
inductive load
U3a
R7 47k
mosfet
R12 100k
R11 1k0
R10 100R
R3 0R1
U2c
C3 220n
C4 10n
0V

Fig. 10

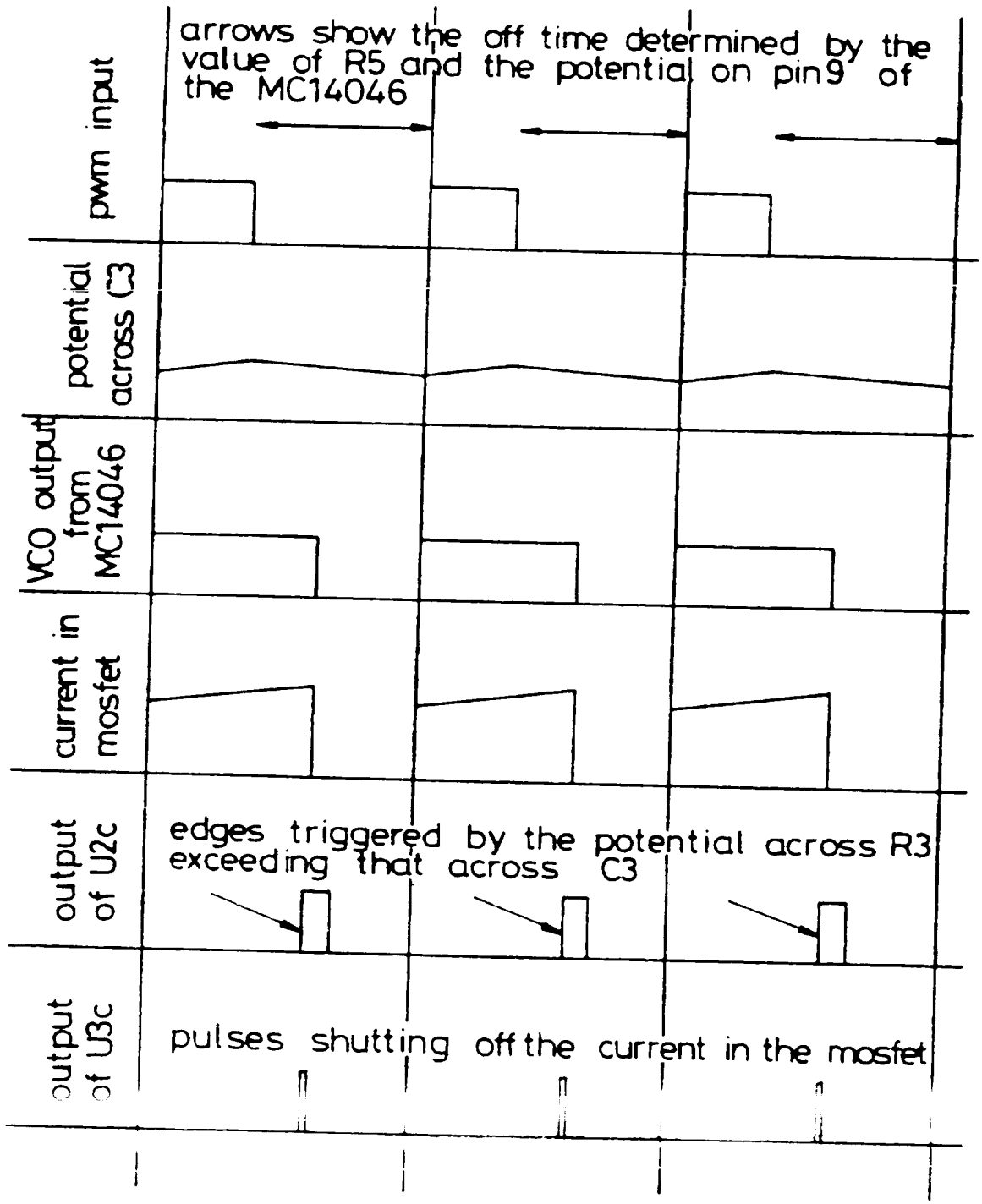

Fig. 11

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A PHASE LOCKED LOOP CURRENT CONTROL CIRCUIT ARRANGEMENT FOR AN INDUCTIVE LOAD

The present invention relates to a phase locked loop current control circuit arrangement for an inductive load.

The electric current in an inductive load supplied from a direct current (dc) source is commonly controlled by switching the supply to the load on and off such that it is on for a variable proportion of the time. This is known as pulse width modulated (pwm) or switch code current control. A typical application would be the control of current flow in an electric solenoid, such as a fuel injector solenoid for an internal combustion engine, for example.

When an electronic system is used to control an analogue parameter, such as current in an inductive load, it is common practice to arrange the system such that it outputs a pwm digital drive signal in preference to a true analogue drive signal. A pwm digital signal is illustrated in figure 1. This is a signal which has a constant repetition rate and conveys information by means of the duty cycle of the signal, i.e. that proportion of the time the signal is high. This type of signal commonly uses standard logic levels where high is nominally 5 volts and low 0 volts, for example. The analogue quantity of the pwm drive signal is therefore represented by its duty cycle and thus, in the case

of current control in an inductive load, current is controlled by varying the duty cycle.

A basic system for controlling current in an inductive load is schematically illustrated in figure 2. This comprises a control system for generating a pwm source signal, a current control circuit arrangement comprising circuit means for processing the pwm source signal (P) to generate a pwm drive signal (Q), and a drive circuit for the inductive load. The control system is typically a low power microprocessor based system operating at standard logic levels of 0 volts and 5 volts, for example. The control system enables the current in a higher power load, operating at vehicle battery voltage (12 volts), for example, to be controlled.

A simple pwm drive circuit is illustrated in figure 3 in which some typical circuit values have been included as examples. In operation, the MOSFET is switched on and off in accordance with the high and low states respectively of the pwm drive signal (Q). When the MOSFET is on current flow through the inductive load rises. However, when the MOSFET is off, current does not drop to zero but continues to flow through the recirculating diode (the potential

The waveforms of figure 4 illustrate how control of current in the inductive load is achieved by the basic system. It can be seen that the control arrangement circuit processes the pwm source signal (P) to provide a drive signal (Q) which is synchronous (positive edge) with the pwm source signal but which has a smaller duty cycle. An increase in the duty cycle would result in an increase in current level in the inductive load. For control of current in inductive loads such as fuel injector solenoids it is desirable to use a control circuit arrangement in which the generated drive signal is synchronous with the source signal.

Known pwm current control circuit arrangements include the "synchronous switch on and current peak switch off" circuit as illustrated in figure 5 and the "constant off-time" circuit as illustrated in figure 6.

The operation of the synchronous switch on and current peak switch off circuit is as follows. The low pass filter filters the pwm source signal to provide an analogue voltage level at G which is proportional to the duty cycle of the pwm source signal. The latch turns on the MOSFET at the start of each cycle of the pwm source signal. When the current in the MOSFET reaches a level such that potential across R_S, a resistor forming a current

pathway with the MOSFET, exceeds that at G the comparator switches the latch, and thus the MOSFET, off. It can be seen from waveform (c) in figure 7 (and from figure 8) that this circuit arrangement, as desired, generates a pwm drive signal which is synchronous with the pwm source signal. Whilst this arrangement could perform the exact function required in the present application, a problem is encountered in that it sub-harmonic oscillates under certain conditions. The problem of sub-harmonic oscillation is discussed in the Motorola data sheet for device UC3842A. The data sheet proposes methods to overcome the sub-harmonic oscillation but these are not normally suitable for the present application.

It will be appreciated from figures 7 and 8 that if the duty cycle of the pwm source signal is changed, the switch off points of the MOSFET are affected but the switch on points remains in synchronisation with the switch on points of the source signal. The switch off points can also be affected if load conditions change, typically because of changes in supply potential (Vbatt in figure 5) as the load resistance changes with temperature. The duty cycle of the pwm drive signal will be changed even though the duty cycle of the pwm source signal remains unchanged.

The operation of the constant off-time circuit (figure 6) is similar to that of the synchronous switch on arrangement. However, in this arrangement, the pwm source signal is not connected to the latch to provide synchronous switch on. In fact, the voltage level at G determines the MOSFET current at which the latch will switch off the MOSFET (in a similar manner to the synchronous switch on arrangement). When the latch is switched off the monostable generator is triggered so that its output goes high a fixed period later and thus switches the latch on again at that time. It should be noted that the off-time periods are fixed but the on-times may vary for reasons similar to those mentioned before in respect of changes in the duty cycle of the pwm drive signal in the synchronous switch on arrangement. The pwm drive signal in this arrangement is not therefore of a fixed period and so can not be synchronised with the pwm source signal. The waveforms (c) and (d) in figure 7 illustrate this point. This circuit arrangement does not, however, suffer from sub-harmonic oscillations.

It is an object of the present invention to obviate and mitigate the problems of the aforesaid prior art circuit arrangements and, in particular, to provide a circuit arrangement for generating a

pwm drive signal for a drive circuit for an inductive load in which the drive signal is synchronous with the source signal and is not affected by sub-harmonic oscillations.

According to the present invention this is achieved by providing a phase locked loop control arrangement for a pulse width modulated (pwm) drive circuit, comprising circuit means for generating a nominally constant off-time pwm drive signal from an inputted pwm source signal, means connected thereto for comparing the phase of the inputted pwm source signal with the phase of a signal in said nominally constant off-time circuit means wherein said means generates a signal representative of the phase difference between the pwm drive signal and the pwm source signal and an output of said phase comparison means is connected to a control input of a generator of said constant off-time circuit means and said phase comparison means outputs a signal to vary the pulse duration of the generator in order to lock the phase of an output signal of the generator with a predetermined point in each cycle of the pwm source signal.

Preferably, the arrangement is such that the

to lock the switch on point of the generator output

with a predetermined point in the cycle of the pwm source signal.

Preferably also, the arrangement is such that the pulse duration of the generator is varied in order to lock the switch on point of the generator output signal with the switch on point of the pwm source signal.

Alternatively, the arrangement is such that the pulse duration of the generator is varied to lock the switch off point of the generator output signal with a predetermined point in the pwm source signal such as the switch off point, for example.

Preferably, the phase comparison means has a first input connected to the pwm source signal input and a second input connected to the output of the generator.

Alternatively, the second input of the phase comparison means may be connected to an output of a voltage comparison means of the nominally constant off-time circuit means, wherein the voltage comparison means, in use, compares a voltage signal level occurring at an output of a low pass filter which connects one of the comparison means inputs with the input for the pwm source signal and a voltage signal level occurring across a resistor which forms a current path with the pwm drive circuit, said voltage signal level occurring across

the resistor being applied to a second input of the comparison means and said comparison means outputs a signal when the voltage signal level across the resistor exceeds that occurring at the output of the low pass filter.

The phase comparison means may comprise the phase comparison section of an MC14046 and the nominally constant off-time circuit means may comprise the oscillator section of the MC14046 operating in monostable mode.

The foregoing and further features of the present invention will be more readily understood from the following description of a preferred embodiment, by way of example thereof, with reference to the accompanying drawings, of which:

Figure 1 is an illustration of a pwm digital signal waveform;

Figure 2 is a schematic block diagram of a basic system for controlling current in an inductive load;

Figure 3 is a circuit diagram of a simple pwm drive circuit forming part of the system of figure 2;

Figure 4 illustrates the waveforms at various points in the basic system of figures 2 and 3;

Figure [illegible] is a schematic block diagram [illegible] known circuit arrangement for controlling current in an inductive load;

Figure 6 is a schematic block diagram of another known circuit arrangement for controlling current in an inductive load;

Figure 7 illustrates the waveforms for the known inductive load current control systems of figure 5 and figure 6 and the circuit arrangement (figure 9) of the invention;

Figure 8 is an enlarged view of a portion of waveform (c) superimposed on waveform (b) of figure 7 but is also illustrative of waveforms in the circuit arrangement (figure 9) of the invention;

Figure 9 is a schematic block diagram of a phase locked loop current control circuit in accordance with the embodiment of the invention;

Figure 10 is an example of a practical circuit layout for the embodiment of figure 9; and

Figure 11 illustrates waveforms at various points in the circuit of figure 10.

The present invention relates to the application of the phase locked loop principle to current control of a pulse width modulated drive circuit driven by a pulse width modulated signal. This provides the advantage that the drive signal is synchronous with the source signal but does not suffer from sub-harmonic oscillation as in the known synchronous switch on and current peak switch off circuit arrangement. In fact, the present invention

is based on another known circuit arrangement, namely the constant off-time circuit. The invention essentially comprises varying the pulse duration of the monostable generator of a constant off-time circuit in order to lock the phase of the output of the monostable with that of an inputted pulse width modulated source signal.

Figure 9 is a schematic block diagram of an embodiment of a phase locked loop current controller in accordance with an embodiment of the invention. This essentially comprises the constant off-time circuit as illustrated in figure 6 but includes a phase comparison means connected between the pwm source signal input and the output of the monostable. The phase comparison means compares the phase of the pwm source signal and, by means of its output connected to a control input of the monostable, controls the pulse duration of the monostable to cause the phase of the monostable output to be locked to a predetermined point in the cycle of the pwm source signal.

The phase locking effect of the phase comparison means can be better understood from a comparison between waveforms (d) and (e) (which refer to the [illegible] refer to the phase locked loop circuit of figure 7. Waveform (d) illustrates the potential across a

current sense resistor in series with the MOSFET (R_S in figure 9) or current in the MOSFET of the constant off-time circuit arrangement of figure 6 where the pulse duration of the monostable, i.e. the off-time, is T_1. It will be appreciated from waveform (d) that the constant feature of the waveform is the fixed off-time (T_1) and that if, for whatever reason, the duty cycle is changed, both the switch on and switch off points will be affected. Thus, this circuit, as previously mentioned, cannot be synchronised with the pwm source signal. However, the inclusion of the phase comparison means allows the pwm drive signal to be synchronised with any point of the pwm source signal. Waveform (f) illustrates positive edge synchronisation of the switch on point of the pwm drive signal with the source signal to provide a waveform which is, in fact, identical to that of the synchronous switch on current peak switch off circuit arrangement of figure 5.

A comparison of waveform (g) with those of (d) and (e) of figure 7 illustrates much the same point but where the pwm drive signal is negative edge synchronised on switch off with the pwm source signal.

Whilst figure 9 illustrates a preferred embodiment of the circuit arrangement of the

invention, it will be understood that there are a number of variations in the circuit which could be made. For example, the input B of the phase comparison means could be connected to the R input of the latch rather than to the output of the generator as illustrated by broken line 10 in figure 9. It is also possible to add a divider chain in the circuit so that the MOSFET switches at a multiple of the pwm source signal frequency rather than having the same switching frequency as is evident from the waveforms of figure 7.

One favourable feature of the circuit arrangement of the invention is that, in the absence of phase locking, it behaves as a constant off-time circuit. This means that when conditions are changing rapidly, normally either the pwm source signal changing or the supply potential to the load changing, current control is neither lost nor subject to sub-harmonic oscillation; the only degradation being a loss of synchronisation between pwm source signal and the pwm drive signal.

The circuit arrangement of the invention can provide for better current control than known circuit arrangements. This can be understood by [illegible] portion of waveform (c) superposed on waveform (b) of figure 7. This illustrates the relationship

between the potential at point G in the circuit of figure 5 (and also figure 9) with the potential across R_S and illustrates the synchronous switch on and current peak switch off principle of said circuit. It will be appreciated that where the duty cycle of the pwm drive signal is changed for whatever reason the switch off point will be affected and the current level at that point will also be affected. This leads to the possibility that the current level in the inductive load fluctuates due to changes in the duty cycle. However, in the case where the circuit arrangement of the embodiment of the present invention utilises negative edge synchronisation, the switch off point can be locked to one point of the cycle and so current is kept constant even when the duty cycle varies.

An example of a practical implementation of the phase locked loop current control circuit is shown in figure 10. The circuit uses the oscillator section of the MC14046 as a nominally constant off-time circuit and the phase comparator section for phase comparison of the pwm source signal with a signal in the nominally constant off-time circuit. However, it will be appreciated that other phase comparators are equally suitable for implementing the invention.

The various features of the circuit can be summarised as follows:

1. R6, R7 and C3 filter the pwm source to an analogue potential in the range 0 to 200 milli volts.

2. R3 senses the current in the MOSFET with a scale of 200 milli volts representing 2 amps.

3. R10 and C4 form a high frequency cut off filter to remove spikes across R3.

4. U2c detects the current peaks exceeding the demand from the pwm source signal.

The action of the MC14046 explains the remainder of the circuit. The relevant points are:

1. The edge sensitive phase detector is used (PC2);

2. R1, R2 and C2 form the low pass filter needed by the phase lock loop;

3. The MC14046 oscillator section is made to function as a monostable; and

4. The output of the MC14046 is buffered directly through three sections of U3 to provide a low impedance drive to the MOSFET gate; this is, again, just by way of example.

The way that the MC14046 behaves as a monostable

points:

1. When acting as a free running oscillator the period is determined by the time it takes to charge C1 to set limits. The charging current to C1 is the sum of two components: the current in R4 and the current in R5.

2. The currents in R4 and R5 can be switched on and off using the open collector comparators U2a & b.

3. When the comparator outputs are low (currents turned on), the current in R4 is constant but the current in R5 is variable according to the potential on pin 9 of the MC14046.

The sequence of operation of the MC14046 is (starting with the condition that the MOSFET has just been turned on) as follows:

1. Pin 4 of the MC14046 must be high; R5 will have zero current; the output of U2c will be low and so R4 will have zero current; and so the output of the MC14046 will stay high indefinitely;

2. The current in the MOSFET will increase and, at a certain level, the output of U2c will go high; this will turn on the current in R4 and start the oscillator action in the MC14046 at high speed (because R4 is small) and pin 4 of the MC14046 will go low;

3. This will turn off the current in R4, turn off the MOSFET and turn on the current in R5;

4. The MC14046 is now in a slow oscillation state with a period determined by the potential on pin 9 (this is the off-time "monostable" action); and

5. Eventually pin 4 of the MC14046 goes high and the cycle repeats.

The circuit of figure 10 is given by way of example only. Changes and variations can be made which still fall within the scope of the present invention.

The operation of the circuit of figure 10 can better be understood with reference to figure 11 which illustrates waveforms at various points in the circuit.

Assuming that the circuit is in a phase locked condition, the pwm input is filtered and attenuated to form the sawtooth waveform, i.e. the potential across C3; and the leading edge of VCO output of the MC14046 is coincident with the leading edge of the pwm input (note that the VCO output signal is called the pwm drive signal in the description of figure 2) The basic sequence of operation is as follows:-

1. The current in the MOSFET comes on when the VCO output comes on and gradually increases until the VCO output goes off which switches off the current in the MOSFET;

2. The potential across the current sense resistor, R3 in figure 10, is proportional to the current in the MOSFET;

3. When the potential across the current sense resistor exceeds that across C3 the output of U2c goes high;

4. When the output of U2c goes high a complicated sequence follows:

Because the VCO output of the MC14046 is also high, the output of U3a goes high;

This pulls the output of U2b low, turns on the current in R4, and starts the oscillator in the MC14046 running fast; and

This quickly causes the output of the MC14046 to go low, which turns off the current in R4, turns on the current in R5 and turns off the MOSFET;

5. With current in R5, but not in R4, the oscillator in the MC14046 is in a "normal" situation. The output is low and the duration of this state is determined by the values of R5 and C1 and the potential on pin 9 (of the MC14046); and

6. When the output of the MC14046 goes high again the cycle is complete and it returns to the beginning (i.e. the state described in stage 1).

The following points should be noted:

a) When the VCO output is on, and the MOSFET is turned on, (as described in stage 1 and, by

inference, stage 6) there is no current in resistors R4 and R5. This means that the oscillator in the MC14046 is stopped; and would stay in this state indefinitely if it were not terminated by the action described in stages 3 and 4;

b) It is because of the state described in (a) that this circuit can be said to use the oscillator section of the MC14046 as a monostable; the stable state is as described in (a);

c) The potential of pin 9 of the MC14046 is controlled by the normal phase locked loop action of the MC14046. This is well documented in the manufacturer's data sheet for this component;

d) It is the phase locked loop action which makes the MC14046 turn on the MOSFET at the same time as the pwm source goes high. This is achieved by connecting the pwm source to pin 14 (of the MC14046) and linking pins 3 and 4 of the MC14046.

Basically the phase locked loop will, if possible, bring the rising edges of the inputs to pins 3 and 14 of the MC14046 into coincidence (or into phase). By connecting these inputs to other parts of the circuit it is possible to change the phase relationship between input and output. This

CLAIMS

1. A phase locked loop control arrangement for a pulse width modulated (pwm) drive circuit, comprising circuit means for generating a nominally constant off-time pwm drive signal from an inputted pwm source signal, means connected thereto for comparing the phase of the inputted pwm source signal with the phase of a signal in said nominally constant off-time circuit means wherein said means generates a signal representative of the phase difference between the pwm drive signal and the pwm source signal and an output of said phase comparison means is connected to a control input of a generator of said constant off-time circuit means and said phase comparison means outputs a signal to vary the pulse duration of the generator in order to lock the phase of an output signal of the generator with a predetermined point in each cycle of the pwm source signal.

2. A phase locked loop control arrangement as claimed in claim 1, wherein the arrangement is such that the pulse duration of the generator is varied in order to lock the switch on point of the generator output with a predetermined point in the cycle of the pwm source signal.

3. A phase locked loop control arrangement as claimed in claim 1 or claim 2, wherein the

arrangement is such that the pulse duration of the generator is varied in order to lock the switch on point of the generator output signal with the switch on point of the pwm source signal.

4. A phase locked loop control arrangement as claimed in claim 1, wherein the arrangement is such that the pulse duration of the generator is varied to lock the switch off point of the generator output signal with a predetermined point in the pwm source signal such as the switch off point, for example.

5. A phase locked loop control arrangement as claimed in any preceding claim, wherein the phase comparison means has a first input connected to the pwm source signal input and a second input connected to the output of the generator.

6. A phase locked loop control arrangement as claimed in any one of claims 1 to 4, wherein the second input of the phase comparison means may be connected to an output of a voltage comparison means of the nominally constant off-time circuit means, wherein the voltage comparison means, in use, compares a voltage signal level occurring at an output of a low pass filter which connects one of the comparison means inputs with the input for the pwm source signal and a voltage signal level occurring across a resister which forms a current path with the pwm drive circuit, said voltage signal

level occurring across the resistor being applied to a second input of the comparison means and said comparison means outputs a signal when the voltage signal level across the resistor exceeds that occurring at the output of the low pass filter.

7. A phase locked loop control arrangement as claimed in any preceding claim, wherein the phase comparison means comprises the phase comparison section of an MC14046 and the nominally constant off-time circuit means comprises the oscillator section of the MC14046 operating in monostable mode.

8. A phase locked loop control arrangement substantially as hereinbefore described with reference to figures 9 to 11 of the drawings.

The Patent Office

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Application No: GB 9422140.5
Claims searched: All

Examiner: Mr.S.SATKURUNATH
Date of search: 26 September 1995

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.N): H3A: ASX, AXX; H3P: PKGW

Int Cl (Ed.6): H03K, H03L

Other: Online: WPI, EDOC, JAPIO, INSPEC

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
A	US4743783 NATIONAL - see especially figures3, 4	1

X Document indicating lack of novelty or inventive step	A Document indicating technological background and or state of the art
Y Document indicating lack of inventive step if combined with one or more other documents of same category	P Document published on or after the declared priority date but before the filing date of this invention
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